Design and Simulation of UART Module with BIST Techninque

Girdhar Gopal , Rashmi Chawla

Abstract— In the life cycle of a VLSI device including VLSI development process, testing is performed at various stages. Testing results into production of defect free device. BIST is a technique that allows a system to test automatically itself. BIST generate test pattern automatically, so it can provide less time as compared to an externally applied test pattern and helps to achieve more productivity at the end. Universal Asynchronous Receiver transmitter (UART) is programmable module that is primarily used for asynchronous serial communication. UART module with BIST technique is designed in verilog HDL and Xilinx is used for synthesis and simulation. This design eliminate need for higher expensive tester and offers promising approach for data exchange with reduced development time and cost.

Index Terms — BIST, LFSR, MISR, Simulation, Synthesis, UART, Xilinx, Verilog HDL

1 Introduction

A UART (Universal aynchronous receiver transmitter) is serial communication programmable module which handle data exchange between processor and peripherals. It handle data conversion between parallel and serial data. Basic UART communication needs only two signal signal lines(TXD,RXD) in order to complete full duplex data communication[1,2,3].
TXD is transmitter side output of UART; RXD is receiver side input of UART. UART serial communication module is divided into three submodule: transmitter, receiver and baud rate generator[3, 4]. Each and every module is responsible for its own task. Failure in any one of module affects overall output of UART.The basic job of UART is converting data from parallel to serial for transmission and serial to paralllel on reception[5]. In actual application, usually only a few key features of UART are needed[6].
Manufacturing processes are extremely complex, inducing manufacturer to consider testability as requirement to assure the reliability and functionality of each of their design circuits. Testing of Integrated circuits(Ics) is important to ensure a high level of quality in product functionality in both commercially produced and privately produced products[6].
Built in self test or BIST is a technique in which parts of a circuit are used to test the circuit. BIST architecture consists of linear feedback shift register (LFSR) ,circuit under test and comparator unit. The objective of BIST is to reduce power dissipation.
Main areas in VLSI are performance, cost, testing, area, reliability and power. The demand for portable computing devices are increasing rapidly.
BIST is DFT(design for testability) methdology aimed at detecting faulty components in a system by incorporating test logic on chip [7]. In this paper, internal diagnostic capabilities are built into UART with help of BIST.
The paper is organised into 5 sections. Section 2 explains BIST architecture . Section 3 explains UART architecture with BIST. Section 4 presents result and section 5 provides conclusion of work.

2 BIST Architecture

VLSI testing problems like test generation problems, input combinatorial problems and the gate to I/O problem are discussed and this motivated the designers to identify reliable test methods in solving these difficuties. An insertion of special test circuitry on the VLSI circuit that allows efficient test coverage is answer to the problem. It is addressed by need of design for testability (DFT) using BIST circuit. BIST is an on-chip test logic that is utilized to test the functional logic of a chip, by itself. With rapid increase in design complexity, BIST has become a design consideration in DFT methods and is becoming more popular in today' s state of art SoCs(system on a chip). A popularly designed BIST is able to offset the cost of added test hardware while at the same time ensuring the reliability, testability and reduces maintenance cost. BIST solution consists of an automatic test pattern generator(ATPG), circuit to be tested, a way to analyse the result and a way to compress the result for simplicity. In BIST, a test logic circuit is incorporated in the chip[8]. The extra circuit generates test patterns, applies them to the inputs and the tests the circuit. This extra circuit increases the chip size but reduces the test cycle time. Fig 1 shows BIST module composition.

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Components of BIST are :

Test pattern generator(TPG) : It is a circuit which is to be tested. It can be a microprocessor or a dedicated circuit. Mostly patten used is pseudorandom pattern.

Circuit under test (CUT) : It is a part of circuit that is to be tested. It can be sequential, combinational or memory.

Test Response Analyser(TPA) : It analyses the value sequence on input and compare it with expected output.

Test controller: It control the test execution, it manages TPG, CUT and TRA.

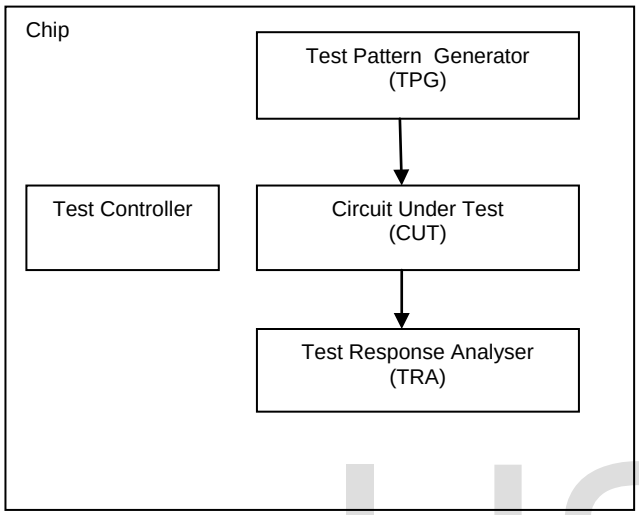


Fig. 1 BIST module composition

2.1 Linear feedback shift register(LFSR)

LFSR is used to generate pseudorandom testvectors in the chip. It is mainly used test pattern generator(TPG). THE output at each stage of an lfsr are used as input of circuit. The LFSR is clocked for a large number of cycles and output is monitored. It is implemented with shift register and Ex-OR gate[9,10]. Fig 2 Shows 8-bit LFSR.

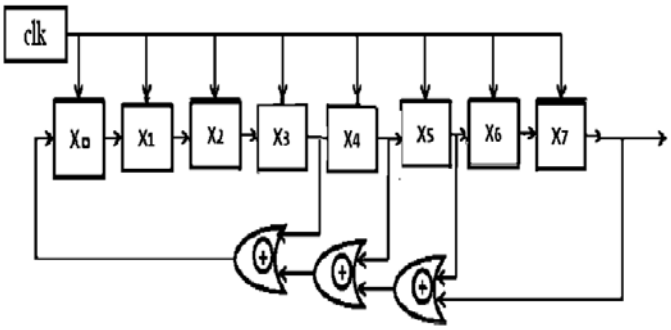


Fig. 2 8-bit LFSR

2.2 Multiple input signature analysis register (MISR)

MISR is one which can be used to reduce the amount of hardware required. MISR is used to compress the mutiple bit stream. The compressed response is referred to as signature of the device under test.its output developes a signature based on the effects of all the bits fed into it [11]. A signature analyser is formed by adding extra XOR gates at input of LFSR[8]. A test input sequence is applied at the input and the resulted output sequence is compared with the signature to determine a faulty circuit. Fig. 3 shows MISR structure.

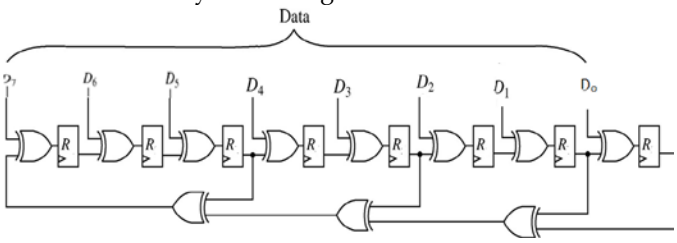


Fig. 3 MISR structure

2.3 Buit-in block observer(BILBO)

A signature analyser and scan test circuit is combined to form a buit-in block observer (BILBO)[11].

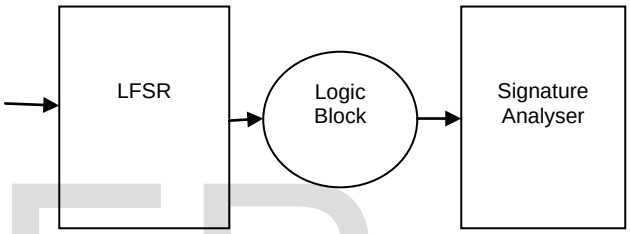


Fig. 4 Blockdiagram of BILBO

Bilbo is a scan register that can be modified to serve as a state register, a pattern register or a shift register.

TABLE 1
BILBO OPERATING MODES

s1	s0	Operating Mode
0	0	Shift Register
0	1	LFSR
1	0	Normal
1	1	MISR

3 UART ARCHITECTURE WITH BIST

UART frame format or serial package consists of start bit , input data , optional parity bit and stop bit. Fig. 5 shows frame format or serial package(excluding parity bit) [12].

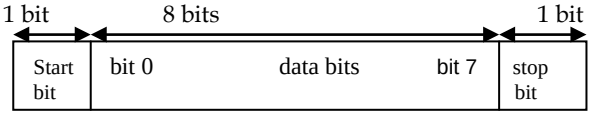


Fig. 5 UART serial Package(excluding parity bit)

UART frame is decided initially and then communication process is started[13,14]. UART serial communication module is divided into three submodule: transmitter, receiver and baud rate generator[14]. Fig. 6 shows UART Block Diagram. Each and every module is responsible for its own task. Failure in any one of module affects overall output of UART.The basic job of UART is converting data from parallel to serial for transmission and serial to paralllel on reception[15,16].

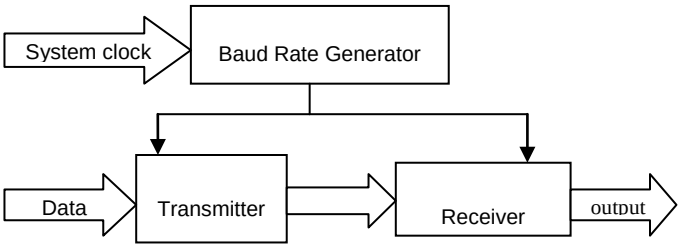


Fig. 6 UART Block Diagram

The basic job of UART is converting data from parallel to serial for transmission and serial to paralllel on reception[16]. Fig. 7 Shows block diagram of UART with BIST. There are three essential components of UART : transmitter , receiver and tester.

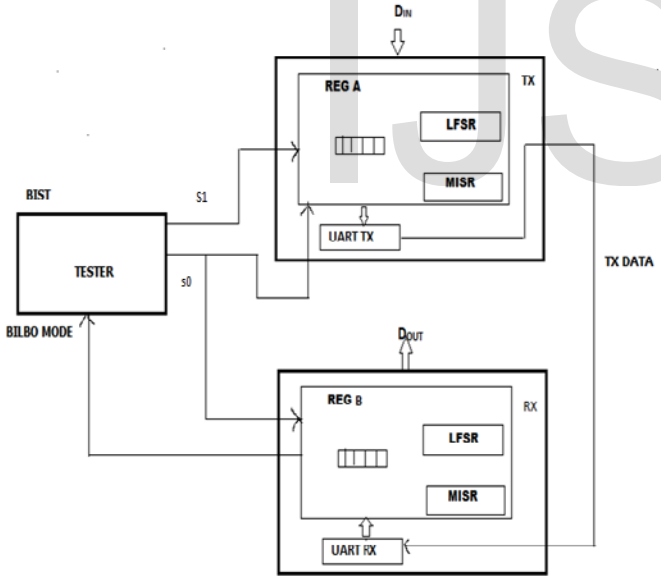


Fig. 7 block diagram of UART with BIST

The function of transmitter module is to convert the 8-bit parallel data into serial data, addition of start bit at the head of data as well as parity bit and stop bit at the end of data.The function of receiver module is to convert serial data into 8-bit parallel data. Receiving unit is responsible for sampling the incoming data and extracting the symbol from the received frame of bits [17].

Baud rate generator is actually a frequency divider. It generate pulse of one cycle periodically, according to baud rate configured [17]. Typical baud rate values are 300, 600, 1200, 2400, 4800, 9600, 19200, 38400, 57600,115200.

4 Synthesis And Simulation Results

Xilinx ISE is (Integrated software environment) is a software tool produced by Xilinx for synthesis and analysis of HDL designs, which enable the developer to synthesize their design , perform timing analysis, examine RTL diagram , simulate a design's reaction to different stimuli and configure target device with programmer.

4.1 RTL View

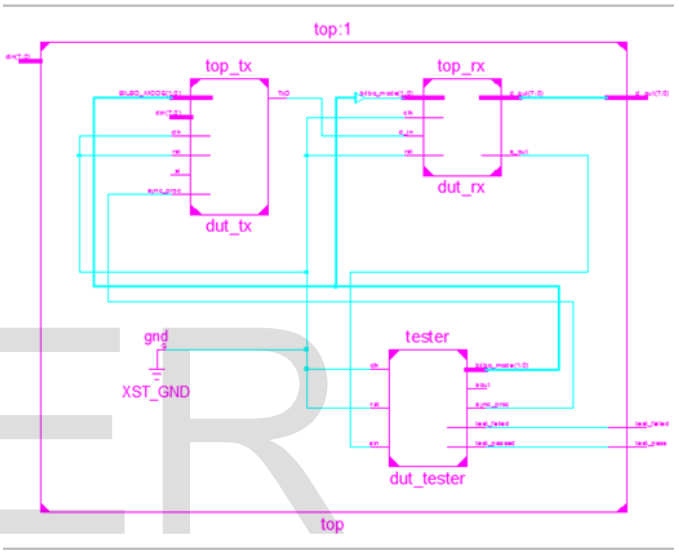


Fig. 8 RTL View of Top Module

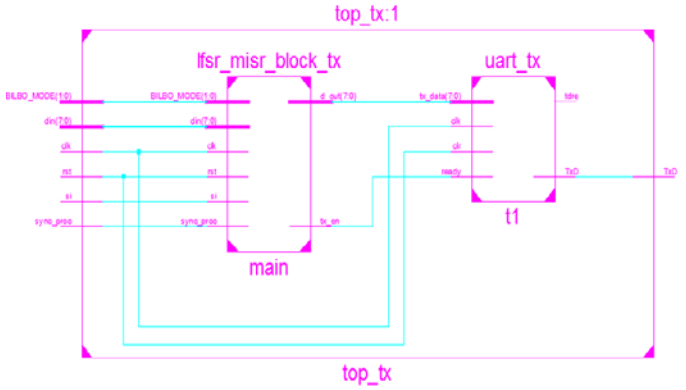


Fig. 9 RTL View Of Top Transmitter

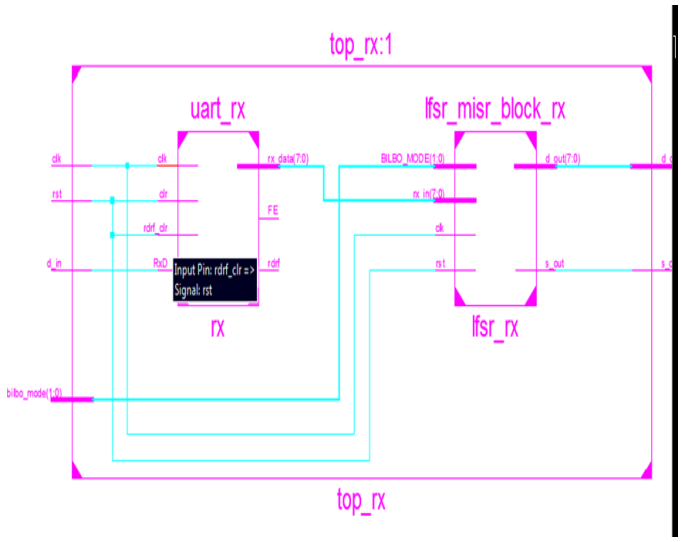


Fig.10 RTL View of Top Receiver

4.2 Simulation of transmitter

The simulation shows the transmission of an 8- bit UART frame format with 1 stop bit and without a parity bit. The transmission was set at 115.2 Kbps using 40MHz clock, which is equal to 25ns(1/40MHz = 25ns Fig. 9 shows the transmission of 8-bit data ("10011111") via DATA[7:0]. The transmitted Uart frame format can be observed at TXD (1 low start bit, 8 data bits and 1 high stop bit).

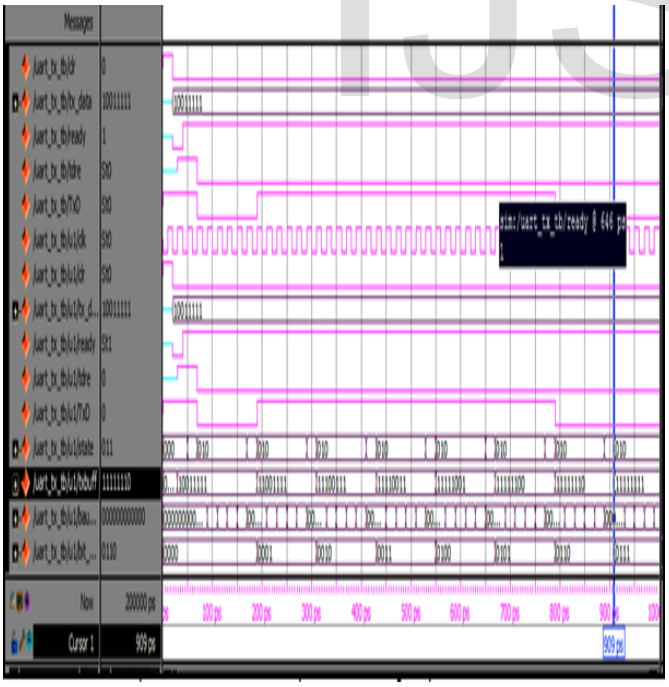


Fig. 11 Transmitter Simulation

4.3 Simulation of Receiver

Fig. 13 shows how an 8-bit serial data from RXD is received.

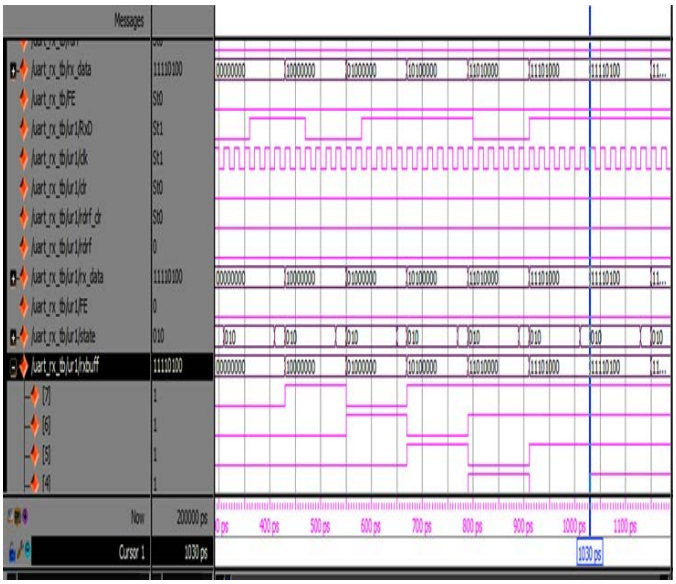


Fig. 12 Receiver Simulation

4.4 Simulation of UART with BIST

FIg.14 shows simulation of UART with BIST

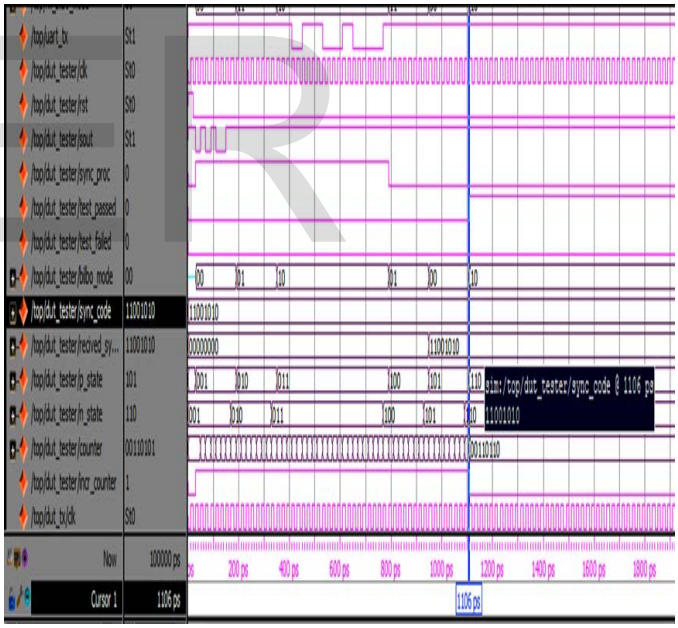
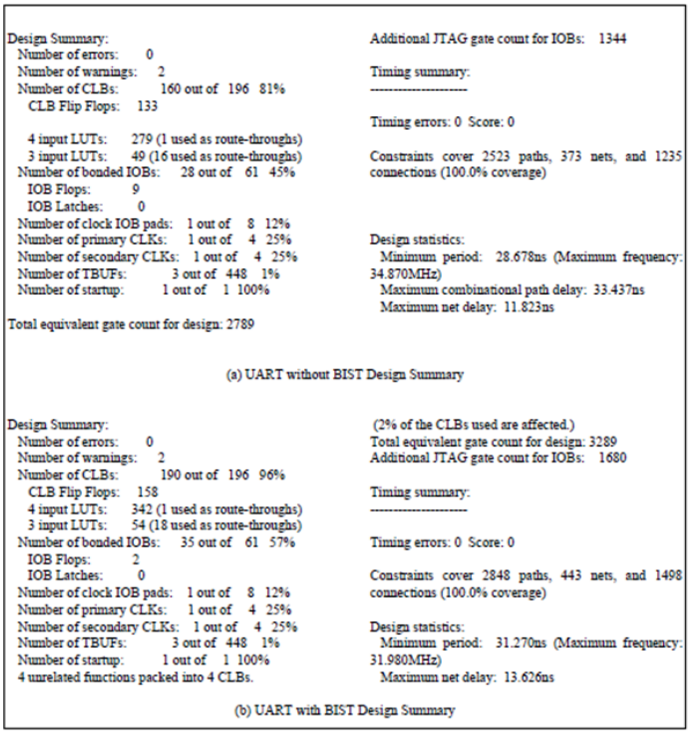


Fig. 13 UART Simulation with BIST

4.5 Design Summary of UART

The report after optimization process will be used as basis for comparison of UART design before and after implimentation of BIST technique.



Design Summary:
Number of errors: 0
Number of warnings: 2
Number of CLBs: 160 out of 196 81%
CLB Flip Flops: 133
4 input LUTs: 279 (1 used as route-throughs)
3 input LUTs: 49 (16 used as route-throughs)
Number of bonded IOBs: 28 out of 61 45%
IOB Flops: 9
IOB Latches: 0
Number of clock IOB pads: 1 out of 8 12%
Number of primary CLKs: 1 out of 4 25%
Number of secondary CLKs: 1 out of 4 25%
Number of TBUFs: 3 out of 448 1%
Number of startup: 1 out of 1 100%
Total equivalent gate count for design: 2789

Additional JTAG gate count for IOBs: 1344
Timing summary:
Timing errors: 0 Score: 0
Constraints cover 2523 paths, 373 nets, and 1235 connections (100.0% coverage)
Design statistics:
Minimum period: 28.678ns (Maximum frequency: 34.870MHz)
Maximum combinational path delay: 33.437ns
Maximum net delay: 11.823ns

(a) UART without BIST Design Summary

Design Summary:
Number of errors: 0
Number of warnings: 2
Number of CLBs: 190 out of 196 96%
CLB Flip Flops: 158
4 input LUTs: 342 (1 used as route-throughs)
3 input LUTs: 54 (18 used as route-throughs)
Number of bonded IOBs: 35 out of 61 57%
IOB Flops: 2
IOB Latches: 0
Number of clock IOB pads: 1 out of 8 12%
Number of primary CLKs: 1 out of 4 25%
Number of secondary CLKs: 1 out of 4 25%
Number of TBUFs: 3 out of 448 1%
Number of startup: 1 out of 1 100%
4 unrelated functions packed into 4 CLBs.

(2% of the CLBs used are affected.)
Total equivalent gate count for design: 3289
Additional JTAG gate count for IOBs: 1680
Timing summary:
Timing errors: 0 Score: 0
Constraints cover 2848 paths, 443 nets, and 1498 connections (100.0% coverage)
Design statistics:
Minimum period: 31.270ns (Maximum frequency: 31.980MHz)
Maximum net delay: 13.626ns

(b) UART with BIST Design Summary

Fig. 14 Design Summary of UART

5 Conclusion

This design uses Verilog as the design language to achieve the module of UART and Xilinx ISE 14.7 for simulation and testing. Result are stable and reliable which shows correct functionality. With implimentation of BIST, expensive testing requirements are eliminated. The design has greater flexibility, error free data exchange.

Acknowledgement

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References

[1] Fang Yi-Yaun, Chen Xue-jun, "Design and Simulation of UART Serial Com-minacation Module Based on VHDL", Shanghai University of Engineering and Science, 2011.

[2] Liakot Ali, RoslinaSidek, IshakAris, AlauddinMohd. Ali, and Bam-bangSunaryo, "Design of a micro- UART for SOC application", Computer and Electrical Engineereingvol 30, pp.257-268.

[3] L. K Hu and Q.CH. Wang, "UART-based Reliable Communication and performance Analysis", Computer Engineering Vol 32, Dec 2006, pp. 247-249

[4] Amanpreet Kaur, Amandeep Kaur, "An Approach For Designing A Universal Asynchronous Receiver Transmitter (UART)", IJERA Vol. 2, Issue 3, May-Jun 2012, pp. 2305-2311.

[5] A Review on Serial Communication by UART" Ms.Neha R. Laddha , Student and Prof. A. P. Thakare Head of the Department of Electronics and Telecommunication Sipna's COET, A Amravati (MS) INDIA. Volume 3, Issue 1, January 2013 ISSN: 2277 128X International Journal of Advanced Research in Computer Science and Software Engineering.

[6] Dr. Garima Bandhawarkar Wakhle, Iti Aggarwal and Shweta Gaba," Synthesis and Implementation of UART using VHDL Codes", International Symposium on Computer, Consumer and Control, 978-0-7695-4655-1/12© 2012 IEEE DOI10.1109/IS3C.2012.10

[7] Bibin M C, Premananda B S, "Implementation of UART with BIST Technique in FPGA" International Journal of Inventive Engineering and Sciences (IJIES). ISSN: 2319– 9598, Volume-1, Issue-8, July 2013.

[8] Huimei Yuan, Junyou Yang,Peipei Pan," Optimized Design of UART IP Soft Core based on DMA Mode" 978-1- 4244 -5046-6/10 2010 IEEE.

[9] Mohd Yamani Idna Idris, Mashkuri Yaacob, Zaidi Razak, "A VHDL implementation of UART design with BIST capability" Malaysian Journal of Computer Science, Vol. 19 (1), 2006.

[10] Shouqian Yu,Lili Yi ,Weihai Chen,Zhaojin Wen," Implementation of a Multi-channel UART Controller Based on FIFO Technique and FPGA" 1-4244-0737-0/07/$20.00 c 2007 IEEE.

[11] Mahat N.F, "Design of a 9-bit UART module based on Verilog HDL", in the proceedings of 10th IEEE International Conference on Semiconductor Electronics (ICSE), 19-21st Sept. 2012, DOI: 10.1109/SMElec.2012.6417210, pp. 570-573.

[12] Girdhar Gopal, Sangeeta Dhall, "Design and simulation of UART Serial Communication Module" International Conference on Sustainable Development through Research in Engineering and Management , Dec. 26-27, 2016

[13] Dr.T.V.S.P. Gupta, Y. Kumari, M.Asok Kumar "UART realization with BIST architecture using VHDL" International Journal of Engineering Research and Applications (IJERA) ISSN: 2248-9622 www.ijera.com Vol. 3, Issue 1, JANUARY-February 2013, pp. 636-640

[14] Naresh patel, Vatsalkumar Patel and Vikaskumar Patel "VHDL Implementation of UART with Status Register" 2012 International Conference on Communication Systems and Network Technologies(IEEE).

[15] Hazim Kamal Ansari, Asad Suhail Farooqi," Design Of High Speed Uart For Programming FPGA" International Journal Of Engineering And Computer Science Volume1, Issue 1, Oct 2012.

[16] Shikha Kakar, Balwinder Singh and ArunKhosla,"Implementation of BIST Capability using LFSR Techniques in UART", in the proceedings of International Journal of Recent Trends in Engineering, Vol 1, May 2009, No. 3.

[17] Bhavna manure and Rahul tanwar, "UART with automatic baud rate generator and frequency divider" Journal of Information Systems and Communication on 15feb 2012.